Challenges Related to Memory Cluster Tests
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Background Test and Philosophy

• Industry desires:
  – Identify issues at the earliest possible stage of a test program
  – Diagnostics to pin point and resolve issues
  – Low cost testing
  – High test coverage
  – Reuse of test software, equipment, automation etc.
Background Test and Philosophy

• Design for Testability (DFT)
  – Method/process to assure industry desires
  – Requires discipline, analysis and buy-in
  – Test and Equipment expertise up front on design
  – Design hooks required to allow capability
  – Target 90% or higher coverage
Background Test and Philosophy

• DFT Reality:
  – Designers do not like adding circuitry
  – Designers do not want testability driving design
  – Limitations may be driven by requirements
  – Methods require hooks to allow test mode
  – Test methods at times increase initial cost
  – Conventional methods, boundary scan, In-Circuit Test (ICT) etc. much more complex with advances in technology
Background Test and Philosophy

• Options for test coverage
  – Functional Test
  – Boundary Scan, ICT or a combination
  – Other: P1581
Memory Test Approaches (Board/System)

• Functional Test
  – Memory functional dependant on control device
  – Timing impacts and interface issues
  – Coding overhead: (8000 to 25000 SLOC)
    • SLOC - Single Lines of Code
      – Code complexity, need multiple patterns
      – Timing and sequences vary based on technology
Memory Test Approaches (Board/System)

• Functional Test
  – Test resource control access required
  – Design must be well thought out up front
  – Operating system impacts
  – Internal network impacts to sequencing
  – Memory sequence and test duration impacts
Memory Test Approaches (Board/System)

- **Boundary Scan**
  - BSDL file accuracy dependent on vendor
  - Tool knowledge and compatibility
  - Vector count and length increases complexity
  - Serial technology increases test time
  - Long paths increase maintenance/debug time
  - Some memory technologies non-compliant
• ICT
  – Fixtures drive overall cost and complexity
  – Decreasing technology sizes cause access and coverage issues
  – Need ability for board control
  – Processor must be stopped for memory control
  – Dual-sided boards, ICT increases complexity and cost
  – Noise issues for sensitive boards
  – Design complexity drives abilities to integrate/debug
Memory Test Approaches (Board/System)

• Boundary Scan and ICT Combination
  – Combination allows for increased coverage
  – Many parts do not include boundary scan
  – ICT will aid in cluster test process
  – ICT aids in discrete component verification
  – Clock signals must be controllable
  – Increases test complexity
  – Technology shrinking ---- pin reliability
Memory Test Approaches - Example

- Processor
- Processor Support ASIC
- Flash Memory
- SRAM
- DPSRAM

Connections:
- Processor to Processor Support ASIC: SYSAD Bus
- Processor Support ASIC to Flash Memory: MEM_ADD / MEM_DATA / MEM_CNTL
- Processor Support ASIC to SRAM: ADDR/CNTL
- Processor Support ASIC to DPSRAM: ADDR/CNTL
- JTAG SCAN connection
Memory Test Approaches - Example
Memory Test Approaches (Board/System)

• Other - IEEE P1581
  – No dependence on special design and timing
  – Solution provides full pin level diagnostics
  – May be implemented as part of the build process
  – If components are "known good" will reduce requirements on verification later in cycle
  – Additional features (i.e. device ID etc.)
  – Capability to use in conjunction with other methods
Memory Test Approaches -- Summary

• Many approaches, P1581 is a cost effective solution
• P1581 does not eliminate or replace other methods
• Boundary Scan, ICT viable but usually later in verification cycle
• P1581 increases testability coverage without need for detailed analyses
1581 Food for Thought -- Opinions

- Cost of P1581 logic will pay for itself in benefit to DFT
- P1581 future uses could include version control and verification
- Diagnostic adder -- Selling point for COTS providers
- Good go/no-go verification for test systems
- P1581 could provide argument for reduction of conventional functional testing